Post-CMOS Fabrication Technology Enabling Simultaneous Fabrication of 3-D Solenoidal Micro-Inductors and Flexible I/Os

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***Abstract*— In this paper, co-fabrication and characterization of micro-inductors with mechanically flexible interconnects (MFIs) as I/Os is presented. A double-lithography and double-reflow process is used to obtain different heights of reflowed photoresist domes for the micro-inductors and the MFIs. The developed process allows fabrication of MFIs with different heights, pitches, and materials. The fine-pitch copper MFIs allow for dense connections between chips using interconnect bridging or stitching technologies (embedded multi-die interconnect bridge, heterogeneous interconnect stitching technology, etc.), while the large nickel tungsten (NiW) MFIs enable connections with the base substrate. The interconnect stitch chip can also host integrated passive devices, allowing close integration with active chips. Furthermore, the stitch chip can be fabricated out of low-loss substrate, enabling high-quality passives along with low-loss electrical interconnections. Copper micro-inductors with two different numbers of turns were fabricated on glass to minimize substrate losses; inductance, resistance, and Q-factor values of 0.45 nH, 4 Ω, and 25 were obtained at 33 GHz for the five-turn inductor with a self-resonant frequency of >40 GHz. The compliance of the fabricated 9-μm-thick Cu MFI was measured to be 1.1 mm/N, while that of the 7- and 10-μm-thick NiW MFIs were measured to be 10 and 2.6 mm/N, respectively.**

***Index Terms*— Flexible interconnects, heterogeneous integration, integrated passive devices, micro-inductors.**

I. Introduction

CHIP I/Os play an integral role in not only providing reliable electrical interconnections, but also the mechanical reliability of the overall system. The mechanical reliability of the I/Os is becoming increasingly critical with a greater trend toward heterogeneous 2.5-D and 3-D integration of disparate substrate materials, which results in coefficient of thermal expansion mismatch and an increased number of off-chip I/O demand [1]–[5]. Flexible interconnects have been widely explored as a suitable replacement for conventional solder bumps and copper pillars as I/Os [6]–[10]. Furthermore, there is also a push toward integrating passives (e.g., inductors and capacitors) on, or in close proximity to, the chips [11] as they are an integral part of the various radio frequency (RF) circuits, including filters, amplifiers, oscillators, and transceivers with applications in the communication, sensing, and power delivery domains [12]–[15]. On-chip inductors of planar structures have been traditionally preferred owing to their ease of fabrication and CMOS compatibility. However, these inductors typically suffer from large substrate losses as well as limited footprint due to a large number of metal interconnects fabricated in the back end of line, resulting in limited inductor performance [16]. The 3-D inductors have been explored to circumvent some of the issues of these planar inductors. Specifically, solenoidal micro-inductors have been preferred as high inductance, and low loss is achievable owing to better magnetic field confinement [17]. However, the additional processing steps and complex fabrication procedures make them less feasible for integration. Moreover, the additional fabrication steps are required to fabricate the needed I/Os for interconnections [18].

In this paper, we present post-CMOS wafer-level co-fabrication of 3-D solenoidal micro-inductors with mechanically flexible interconnects (MFIs) of different materials, pitches, thicknesses, and heights for electrical signaling; the described process allows the simultaneous fabrication of I/Os (MFIs) and micro-inductors, thereby preventing additional fabrication steps. A double-lithography and double-reflow process [19] is utilized to get the differential height photoresist domes for micro-inductors and MFIs; smaller height domes are utilized to fabricate fine-pitch MFIs along with micro-inductors, while the larger domes are used for the coarse-pitch MFIs. The developed process further allows the MFIs to be fabricated using different materials, pitches, and thicknesses giving control over the mechanical and electrical properties of the MFIs. This can be important for heterogeneous integration where I/Os of different pitches, heights, and materials may be required for increased integration flexibility.

Fig. 1 shows a schematic of one such topology leveraging multi-height I/Os [21], [22] and 3-D micro-inductors. As shown in this paper, the high-density stitch chip can be fabricated out of a low-loss substrate allowing high-performance 3-D passives (inductors) along with low-loss, high-density electrical interconnects. The fabrication process enables seamless heterogeneous integration of ICs of different substrate

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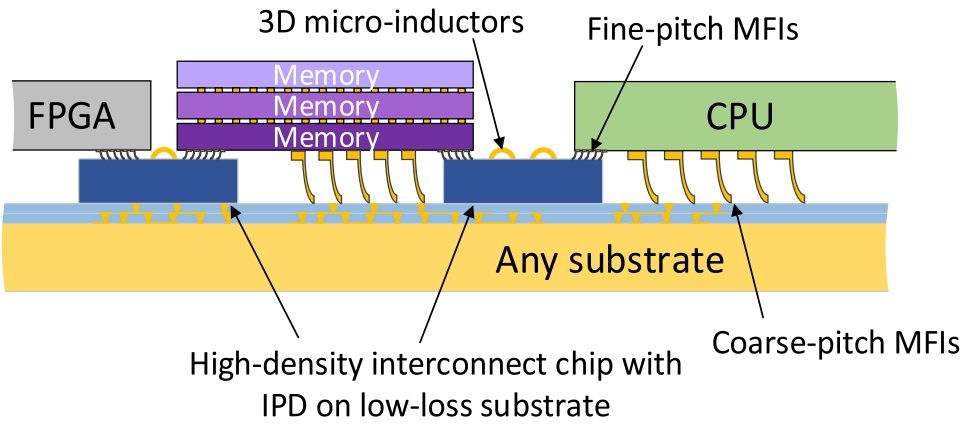

Fig. 1. Envisioned schematic utilizing fabricated micro-inductors and MFIs; figure extends HIST [21], [22].

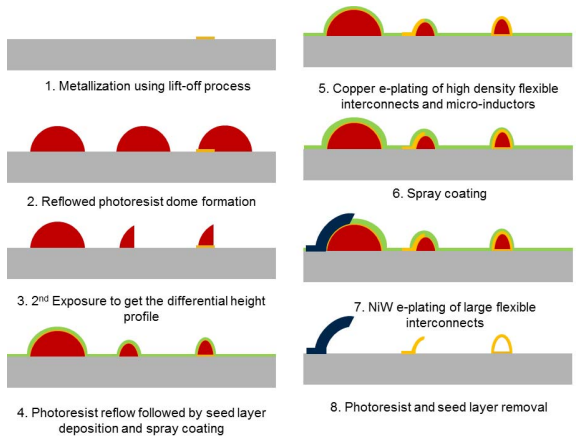

Fig. 2. Fabrication process for micro-inductors and MFIs.

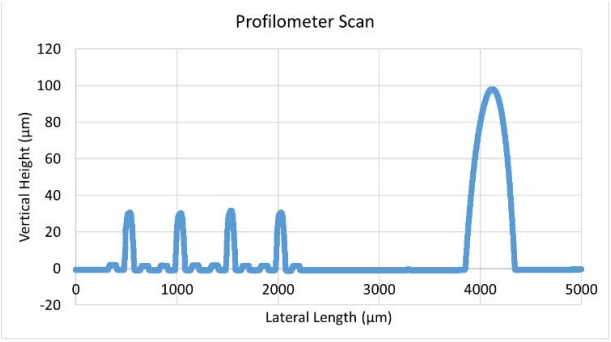

Fig. 3. Profilometer scan of the reflowed domes after double-exposure process—height difference of 70 μm between the small and the large domes was achieved.

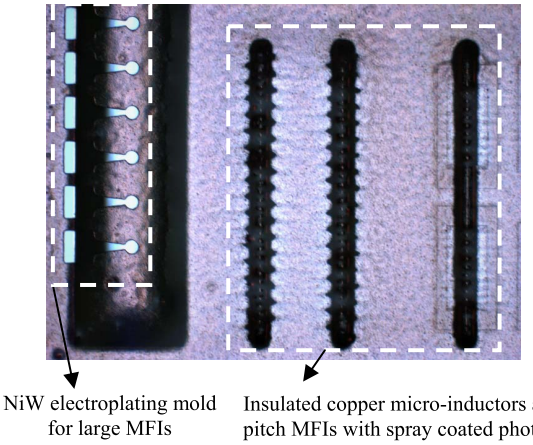

Fig. 4. Optical image showing electroplating mold for large NiW MFIs with resist covered copper micro-inductors and MFIs.

materials utilizing I/Os of different heights, materials, and pitches; fine-pitch Cu MFIs can enable high-density communication between chips using high-density interconnect technologies, including embedded multi-die interconnect bridge [20] and heterogeneous interconnect stitching technology (HIST) [21], [22]. The coarse-pitch nickel tungsten (NiW) MFIs can provide the necessary interconnection between the bottom substrate and the chips while providing a greater vertical elastic range of motion, owing to the higher yield strength of NiW as compared to Cu [23] to compensate for height differences and surface nonplanarities.

II. Fabrication

The co-fabrication process of the MFIs and the micro-inductors is outlined in Fig. 2. A Ti/Cu/Au, with a thickness of 50/2000/100 nm, metallization using a lift-off process is obtained to get the base metallization for the micro-inductors. Large domes are obtained using reflow of thick positive photoresist. A second exposure is then performed, followed by a second reflow process to get the smaller domes [19]. Fig. 3 shows a profilometer scan for the two different dome heights obtained after the second exposure and reflow. A height differential of 70 μm is achieved between the large and the small domes. The height differential between the domes can be modulated by changing the width of the photoresist being exposed in the second exposure. Copper electroplating of small MFIs and micro-inductors is then performed using a spray-coated electroplating mold. After the copper electroplating, a second layer of spray-coated photoresist is applied to isolate the copper-plated structures and create a new electroplating mold for the large MFIs. An optical image of the spray-coated copper micro-inductors and fine-pitch MFIs and the electroplating mold for the NiW MFIs is shown in Fig. 4. NiW is used to electroplate the large MFIs allowing for larger vertical elastic deformation than copper [23]. Seed layer and photoresist are then removed to obtain freestanding structures.

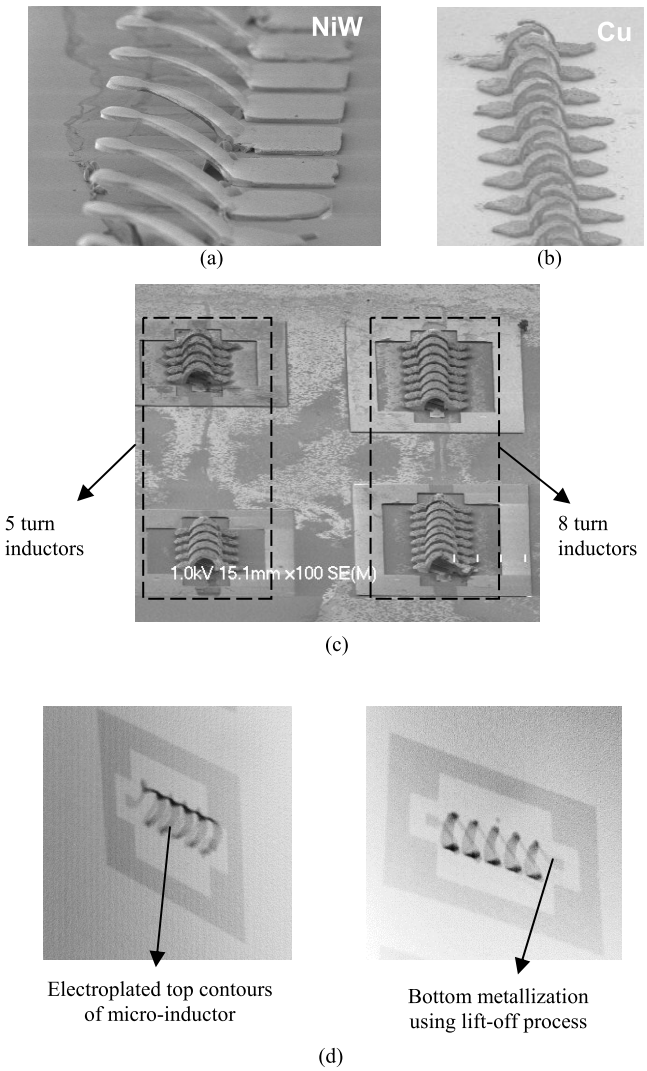

Fig. 5. SEM images of fabricated sample of (a) NiW MFIs, (b) fine-pitch Cu MFIs, and (c) Cu micro-inductors. (d) X-ray images of top and bottom metallization with good connection.

Fig. 5 (a)–(c) shows the SEM images of the fabricated sample with Cu micro-inductors and fine-pitch MFIs and NiW coarse-pitch MFIs. X-ray images of the fabricated five-turn micro-inductor, shown in Fig. 5(d), show a good connection between the top and bottom metallization. SEM images in Fig. 6 show the height difference between the MFIs and the micro-inductors fabricated on the same substrate. The height differential allows heterogeneous integration with micro-inductors embedded between substrate tiers, while MFIs provide the required electrical interconnections.

III. Electrical and Mechanical Measurements

This section presents electrical and mechanical measurements of the fabricated micro-inductors. The RF measurements of micro-inductors were performed to extract their inductance and Q-factors. The fabricated micro-inductors are measured using a Cascade microprobe station and a Keysight PNA X N5245 network analyzer. Prior to the measurements, short-open-load-through calibration was performed up to 40 GHz using a calibration substrate. After calibration, ground-signal-ground (GSG) probes of a 200-μm pitch were

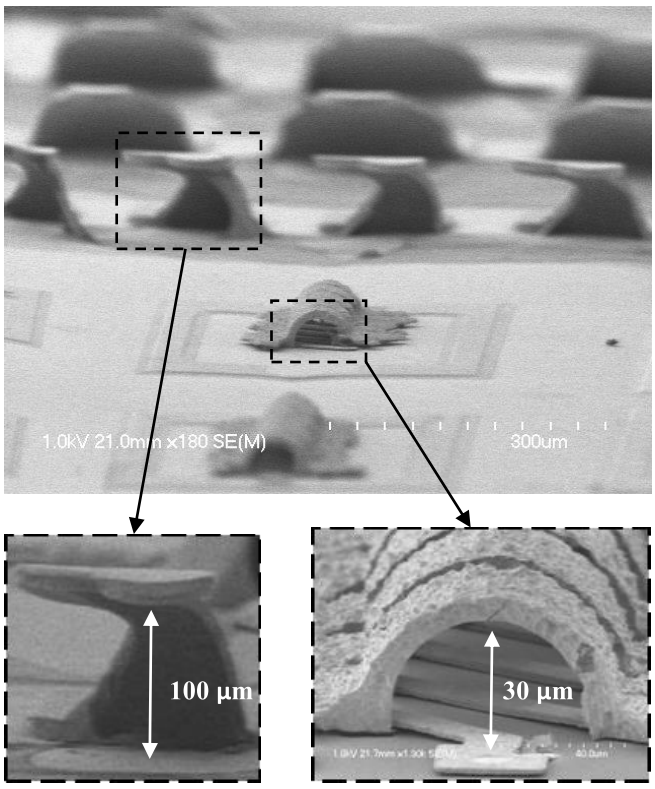

Fig. 6. SEM images of the samples depicting height differential—the height differential between the co-fabricated MFIs and the micro-inductors allows the inductors to be embedded between tiers in a stack, while the MFIs provide the required interconnection and compensate any surface nonplanarity.

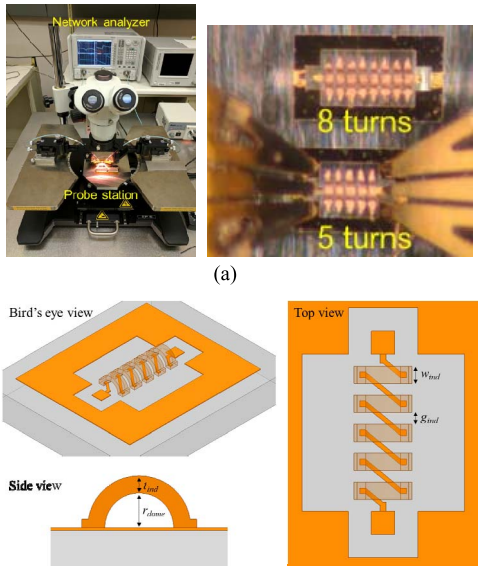

Fig. 7. (a) Measurement setup: A Cascade microprobe station and Keysight network analyzer and optical image of micro-inductors with GSG probes. (b) Simulation configuration for inductors using ANSYS HFSS software; t_{ind}, w_{ind}, and g_{ind} refer to the thickness, width, and gap of solenoid inductors, respectively, and r_{dome} refers to the radius of a sacrificial photoresist dome.

used for two-port measurements, as shown in Fig. 7(a). Each micro-inductor is surrounded by a ground plane to facilitate probing. Fig. 7(b) illustrates simulation configurations

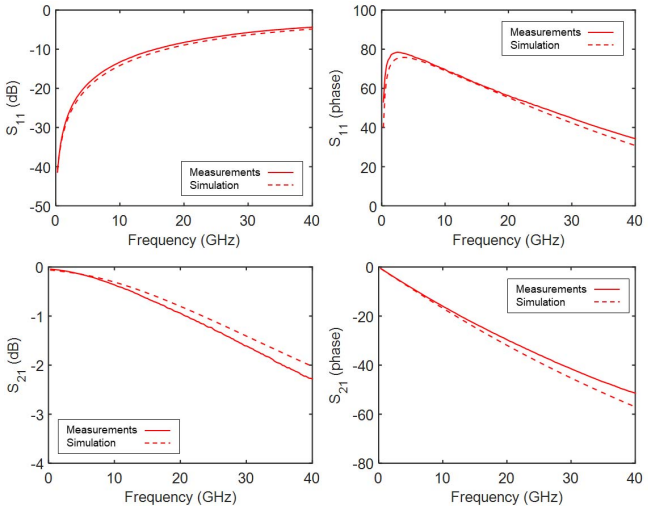

Fig. 8. Measured and simulated S-parameters for the five-turn inductor; results show close match between the simulated and measured values.

for solenoid micro-inductors using full-wave electromagnetic software (ANSYS HFSS, Version 18.1).

Fig. 8 illustrates the measured and simulated S-parameters for the fabricated five-turn micro-inductor. Fig. 8 shows a good match between the simulated and the measured structures. After S-parameter-to-Z-parameter conversion, the resistance, inductance, and Q-factor of each inductor can be extracted using the following equations [24], where Re and Im stand for real and imaginary parts, respectively, and ω is the angular frequency:

$$Z_{\text{diff}} = Z_{11} - Z_{12} - Z_{21} + Z_{22} \quad (1)$$

$$R = \text{Re}(Z_{\text{diff}}) \quad (2)$$

$$L = \text{Im}(Z_{\text{diff}})/\omega \quad (3)$$

$$Q = \text{Im}(Z_{\text{diff}})/\text{Re}(Z_{\text{diff}}). \quad (4)$$

Fig. 9 shows the extracted inductance, resistance, and Q-factor for the five- and eight-turn micro-inductors from the RF measurements. For each structure, five measurement results were averaged with the error bars of one standard deviation. As the number of turns increases, the inductance values increase while Q-factors decrease. The maximum Q-factor of ~25 is achieved at 33 GHz for the 30-μm-radius and 10-μm-thick five-turn micro-inductor. Table I shows the performance comparison of the fabricated inductor with some of the published work for 3-D solenoid-shaped inductors. The fabricated micro-inductors, which demonstrate proof of concept, exhibit a Q greater than 15 for a frequency band of over 35 GHz with a self-resonant frequency of >40 GHz and an inductance of 0.45 nH; the fabricated micro-inductors were not optimized. The fabrication process uniquely allows co-fabrication of I/Os with the micro-inductors; this significantly reduces the number of fabrication steps and increases the ease and flexibility of heterogeneous integration.

The effect of coil radius (r_{dome}) on the Q-factor was also studied using the simulation configuration described earlier. The maximum Q-factor shows an increase with the increase in the coil radius; this is primarily due to lower flux leakage and reduced parasitic capacitance between the base metallization

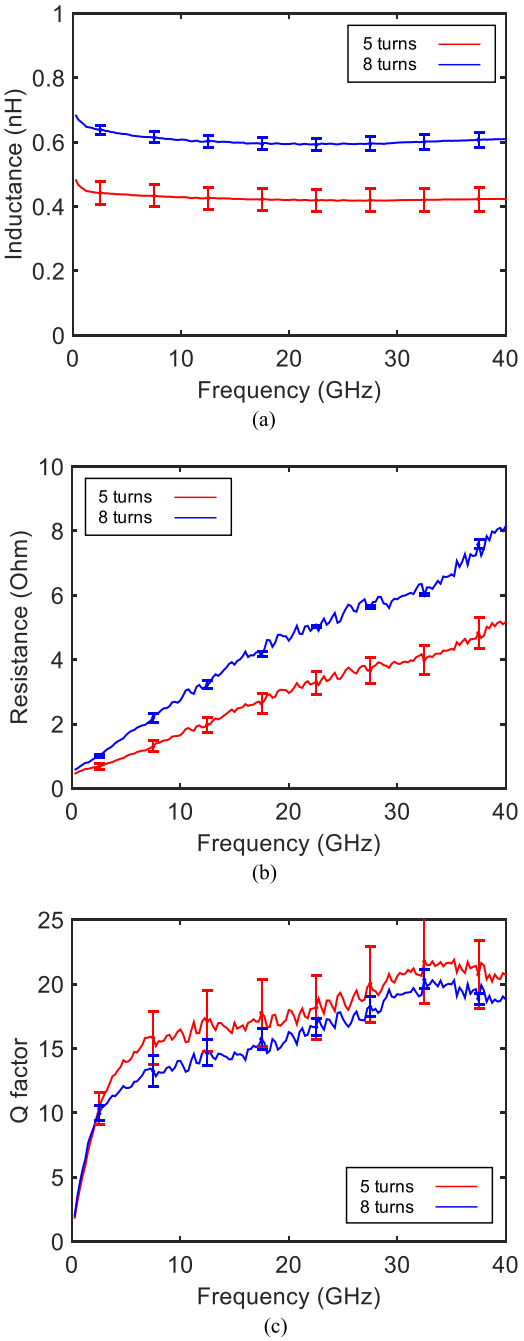

Fig. 9. Measured (a) inductance, (b) resistance, and (c) Q-factor of the five- and eight-turn micro-inductors.

and the electroplated contours of the micro-inductors [25]. The inductance also increases with an increase in coil radius due to a larger core area. The simulation results for this tradeoff are depicted in Fig. 10.

The developed co-fabrication process also gives control over the type of material and thickness of the electroplated layer. This allows modulation of mechanical properties of the MFIs (compliance, elastic range, etc.) to better meet the varying requirements of electronic systems. For example, the total "clamping" force required to maintain a good electrical connection would be a function of the number of I/Os and the compliance of the I/Os. Thus, modulating the compliance can allow for achieving the desired clamping force for a given

TABLE I
PERFORMANCE COMPARISON OF THE FABRICATED INDUCTOR WITH PUBLISHED WORK

Reference	Peak Q @ (f_{qmax})	Frequency Band with Q > 15 (GHz)	L (nH)	SRF (GHz)	Substrate	Inductor shape	Co-fabrication with I/Os
[18]	100 (3.2 GHz)	< 8	3.5	n/r	Glass	3D solenoid	No
[26]	17.5 (70 MHz)	< 0.1	60	n/r	Silicon	3D toroidal	No
[27]	46 (400 MHz)	n/r	38	n/r	Glass	3D solenoid	No
[28]	50 (6 GHz)	< 7	2.3	> 20	Silicon	3D solenoid	No
[29]	32 (0.95 GHz)	< 0.5	1000	1.24	Polymer	3D solenoid	No
This Work	25 (33 GHz)	> 35	0.45	> 40	Glass	3D solenoid	Yes

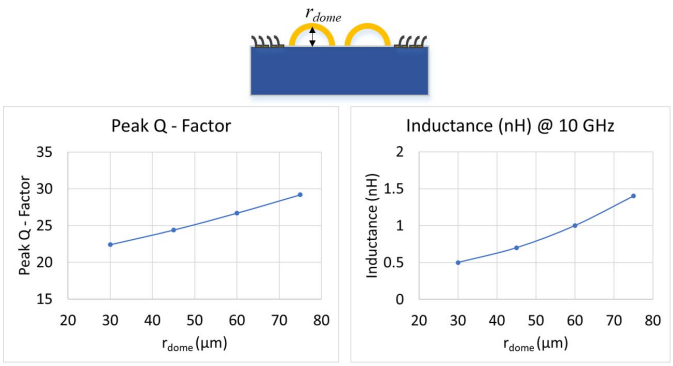

Fig. 10. Tradeoff between dome radius and the micro-inductor's peak Q-factor and inductance.

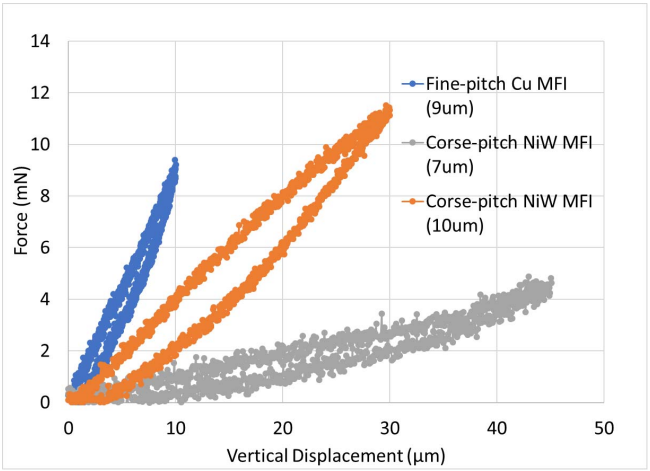

Fig. 11. Compliance measurements for the fabricated MFIs.

number of I/Os. Fig. 11 shows the mechanical indentation results for the fabricated MFIs. The indentation was performed using a Hysitron Triboindenter with a cono-spherical probe tip. The measured compliance of the fine-pitch Cu MFIs with a thickness of 9 μm was 1.1 mm/N, while that of the 7- and 10-μm-thick large coarse-pitch NiW MFIs was 10 and 2.6 mm/N, respectively.

IV. CONCLUSION

In this paper, co-fabrication of 3-D solenoidal micro-inductors and MFIs as I/Os is presented. The developed process enables I/Os to be fabricated with different pitches and vertical heights, enabling seamless heterogeneous integration for RF systems. A maximum height difference of 70 μm was achieved between the large MFIs and the micro-inductors. This large height differential between the micro-inductors and the MFIs can enable embedding of micro-inductors between substrates for 2.5-D or 3-D integration. Fabrication of micro-inductors on the high-density stitch chip allows leveraging low-loss substrates for high-performance passives and low-loss electrical interconnects. The process also gives control over the mechanical characteristics of the fabricated MFIs by allowing multi-material and multi-thickness electroplating processes. Electrical measurements of two different fabricated inductor structures are also presented.

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